IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/690,121	§		
Filed: October 20, 2003	§	Examiner:	Dang, Khahn
Inventor(s):	§	Group/Art Unit:	2111
Le et al.	§	Atty. Dkt. No:	6000-10201
Title: MAPPING OF HOT-SWAP STATES TO PLUG-IN UNIT STATES	§		

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Stephen J. Curran
Printed Name

Signature

September 26, 2006
Date

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Respectfully submitted,

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal filed July 27, 2006, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The present application is owned by Sun Microsystems Inc. An assignment of the present application to the owner is recorded at Reel 014991, Frame 0559.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellant.

III. STATUS OF CLAIMS

Claims 1-23 are pending. Claims 1-23 are rejected under 35 U.S.C. § 102(e). It is these rejections that are being appealed. A copy of claims 1-23 is included in the Claims Appendix attached hereto.

IV. STATUS OF AMENDMENTS

No unentered amendment to the claims has been filed after final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method and system that are adapted to manage the mapping of hot-swap states of a CPCI card from one system to another system. More particularly, embodiments of the present invention can be implemented with CPCI systems that support hot-swappable node and/or I/O cards. The PCI Industrial Computer Manufacturers Group (PICMG) Hot-Swap/High-Availability (HA) specification (e.g., PICMG 2.0 R3.0 or PICMG 2.1 R2.0), which allows the powering-up/down of the card by the hot-swap controller, defines, among other things, that all CPCI slots are controlled individually with states that control the insertion of a hot-swappable card into a slot of the backplane. The states are identified in PICMG specifications. For example, the PICMG hot-swap states, as specified in the Hot-Swap

Specification PICMG 2.1, are 12 states describing the state (or status) of a hot-swap CPCI node card (e.g., Central Processing Unit (CPU) card or an Input/Output (I/O) card).

In one embodiment of the present invention, the CPCI node cards are managed by management ware (or management software) with plug-in units based on the Telecommunication Management Network (TMN) standards. The PICMG states (describing the state of an HA CPCI card) are mapped into a plurality of operation states and available states (or status) for the TMN plug-in units. Accordingly, the management ware having the plug-in units based on the TMN standards can now use these mapped states to manage the state (or status) of the HA CPCI card.

Accordingly, independent claim 1 is directed to a method of mapping a plurality of states for controlling hot-swappability in a Compact Peripheral Component Interconnect (CPCI) system. More particularly, in one embodiment, the method includes specifying a hot-swap state of a CPCI node card. The hot-swap state is for controlling the hot-swappability of the CPCI node card on the CPCI system, for example. Once the hot-swap state has been specified, the method then maps the hot-swap state onto an intermediate state by searching both a common library associated with the CPCI node card and management software for the CPCI node card. Once the hot-swap state has been mapped onto the intermediate state, the method then maps the intermediate state onto a first management state of the management software and a second management state of the management software. The management software requires both the first and second management states to manage the CPCI node card. (See, e.g., Fig. 7; and specification page 3, lines 10-20; page 10, line 22-page 11, line 9; and page 11, line 10-page 12, line 2).

Independent claim 7 is directed to a method that maps at least about 8 or 12 PCI Industrial Computer Manufactures Group (PICMG) states describing the state (or status) of a hot-swap CPCI card into Telecommunication Management Network (TMN) plug-in unit states (e.g., the OperationalState and/or AvailiableStatus states.) The mapping or mappings utilize a Common Operating System Library or Layer (COSL). That is, at first,

the hardware/Operating System (OS) states for the CPCI card are specified in PICMG states in accordance with the PICMG hot-swap specification. The method and system then identifies or defines (explains or interprets) the meaning (e.g., the definition, identification, function, and/or status) of the states on the CPCI card. The method and/or system then maps these states into intermediate states (e.g., COSL state, plug-in unit state or "plugInUnitState"). The intermediate states are then mapped into TMN plug-in unit states (e.g., OperationalState and/or AvailiableStatus). The TMN plug-in unit states corresponding to the hot-swap CPCI card will then comprise the proper identification information for the hot-swap CPCI card, such as plugInUnitType, vendorName, version, etc. Accordingly, the management software (or management ware or management SW) with plug-in units based on the TMN standard can now use these mapped states to manage the state (or status) of the CPCI card. *(See* e.g., specification page 4, lines 1-24; page 11, line 10-page 12, line 2).

Independent claim 10 is directed to a CPCI system that includes a CPCI chassis and a circuit board. The circuit board forms a backplane within the chassis. A CPCI node card is coupled with the circuit board. The node card provides a hot-swap state. A manager manages the CPCI card using a first management state and a second management state. The CPCI system also includes a common library that is associated with the CPCI node card and the manager. The common library provides an intermediate state. The hot-swap state is mapped onto the intermediate state of the common library. The mapped intermediate state is then mapped onto the first and second management states of the manager. *(See* e.g., FIG. 6-8; specification page 3, lines 21-29; page 9, line 16-page 10, line 17; and page 11, line 10-page 12, line 2)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-23 are rejected under 35 U.S.C. § 102(e) as being unpatentable over Larson et al. (U.S. Publication 20030033464) (hereinafter "Larson").

VII. ARGUMENT

First Ground of Rejection:

Claims 1-23 are rejected under 35 U.S.C. § 102(e) as being unpatentable over Larson. Appellant traverses this rejection for at least the following reasons.

Independent claims (by number):

Appellant respectfully submits that claim 1 recites features not taught or disclosed Larson. For example, claim 1 recites features including: " mapping said hot-swap state onto an intermediate state by searching a common library associated with said CPCI node card **and** a management software for said CPCI node card; and mapping said intermediate state onto a first management state of said management software **and** a second management state of said management software ... and wherein said management software requires both said first and second management states to manage said CPCI node card ". Appellant submits these features are not taught or disclosed by Larson.

For reference, Appellant has included a number pertinent portions from Larson:

Larson teaches at paragraph [0016]

> "Server system 100 includes a plurality of cPCI slots 110 for receiving cards/modules 300 (shown in block form in FIG. 3). In one embodiment, system 100 includes ten slots 110 on each side of backplane 106 (referred to as the 10 slot configuration). In an alternative embodiment, system 100 includes nineteen slots 110 on each side of backplane 106 (referred to as the 19 slot configuration)."

Larson discloses at paragraph [0018]

> "In one embodiment, two types of host processor cards 300A may be used

in server system 100--PA-RISC host processor cards and IA32 host processor cards. Multiple host processor cards 300A and hard disk cards 300B are used in embodiments of server system 100, but are each represented by a single card in FIG. 3 to simply the figure. In one form of the invention, up to 8 host processor cards 300A are used in the 10 slot configuration, and up to 16 host processor cards 300A are used in the 19 slot configuration In one embodiment, each of cards 300 can be hot swapped."

Larson also discloses at paragraph [0036]

> "Processor 502 is coupled to FPGA 508. FPGA 508 includes 6 sets of input/output lines 522A-522F. Lines 522A are connected to jumpers for configuring SMC 300E. Lines 522B are hot swap lines for monitoring the hot swap status of cards 300. In one embodiment, hot swap lines 522B include 18 hot swap status input lines, which allow SMC 300E to determine the hot swap status of the host processor cards 300A, hard disk cards 300B, managed Ethernet switch cards 300C and 300D, SMC rear transition modules 300F and 300G, and power supply units 114. Lines 522C are LED lines that are coupled to LEDs 322. Lines 522D are fan input lines that are coupled to fan sensors 306 for monitoring the speed of fans 304. Lines 522E are power supply status lines that are coupled to power supply units 114 for determining whether both, or only one power supply unit 114 is present."

Larson further discloses at paragraphs [0061-0064]

> "The hot swap mode is entered when there is an attempt to remove a card 300 from system 100. In one embodiment, all of the chassis cards 300 can be hot swapped, including SMC 300E, and the two power supply units 114. ....
> [0062] In one embodiment, FPGA 508 includes 18 hot swap status inputs 522B. These inputs 522B allow SMC 300E to determine the hot swap status of host processor cards 300A, hard disk cards 300B, managed Ethernet switch cards 300C and 300D, SMC rear transition module cards 300F and 300G, and power supply units 114. The hot-swap status of the SMC card 300E itself is also determined through this interface 522B.
> [0063] An interrupt is generated and passed to SMC processor 502 if any of the cards 300 in system 100 are being removed or installed. SMC 300E monitors board select (BD_SEL) lines 518 and board healthy (HEALTHY) lines 520 of cards 300 in system 100. In one embodiment, board select lines 518 and healthy lines 520 each include 19 input lines, which are connected to FPGA 508 via input registers 512A and 512B, respectively. SMC 300E monitors the board select lines 518 to sense when a card 300 is installed. SMC 300E monitors the healthy lines 520 to

determine whether cards 300 are healthy and capable of being brought out of a reset state.

[0064] When SMC 300E detects that a card has been inserted or removed, an alarm event is generated. When a new card 300 is inserted in system 100, SMC 300E determines the type of card 300 that was inserted by polling the identification EEPROM 302A of the card 300. Information is retrieved from the EEPROM 302A and added to the hardware fitted table. SMC 300E also configures the new card 300 if it has not been configured, or if its configuration differs from the expected configuration. When a card 300, other than the SMC 300E, is hot-swapped out of system 100, SMC 300E updates the hardware fitted table accordingly."

Larson further discloses at paragraph [0073]

> "A dedicated SMC 300E allows for functionality and integrity tests of the chassis cards 300 without the need of a host processor card 300A or its operating system. Additionally, higher-level management software such as Openview, Network Node Manager, Tivoli, TopTools, and others, can self-discover and fault manage a server system 100 at minimum power and an operational SMC 300E."

The Examiner has asserted and continues to assert Larson teaches each and every element recited in Appellant's claim 1. Specifically, in the detailed action section of the final Office action dated April 24, 2006 the Examiner asserts "the FPGA includes 18 hot swap statuses, and it is clear that a hot swap state of a node card must be correspond to one of the 18 states/statuses of the FPGA associated with the node card and software management so that a hot swap state can be recognized by the FPGA; see at least [0061-0064]; and mapping said intermediate state onto a first management state and a second management state of said management software..." In addition, in the Examiner's response to arguments, the Examiner asserts "The so-called "common library" provided by the FPGA includes 18 hot swap statuses/states provided by the hot-swap status input lines..." The Examiner goes on to assert "See [0036]. Thus it is clear that each swap line includes a plurality of hot swap statuses (states) inputs. As a matter of fact, according to CompactPCI (CPCI) Hot-Swap Specification, hot-swap of a card always involves a plurality of hot-swap states. For example, see Intersil, ..."

The Examiner has indicated further in the Advisory action dated August 7, 2006, that the term "FPGA library" is well-defined in the computer arts and that a simple search

on Google will yield numerous references to the term. Of this, Appellant has no doubt. However, Appellant submits these searches should have enlightened the Examiner to the fact that an "FPGA library" does not refer to a library stored within the FPGA as the Examiner is suggesting. The phrase "FPGA library" typically refers to a library of functions and/or circuit elements from which a circuit/logic designer may choose when designing an FPGA device.

Thus, it appears to Appellant the Examiner is interpreting Larson's 18 hot-swap status input lines as some 18 different hot-swap statuses and thus some "common library" of hot-swap states within the FPGA. Appellant disagrees with this interpretation. Although Appellant understands the Examiner may interpret the claims as broadly as is practicable, Appellant submits that Examiner has erroneously interpreted at least portions of Larson and thus incorrectly applied Larson to Appellant's claims.

From the foregoing disclosures in Larson, Appellant submits the 18 hot-swap input lines are just that; 18 individual wires/lines each with a single input that is associated with a single device (e.g., cards 300). Further, Appellant notes that in the electrical arts, especially as used in board and circuit interconnections, it is well known that a line generally refers to a single wire or single signal path, and NOT that "it is clear that each swap line includes a plurality of hot swap statuses (states) inputs" as the Examiner has suggested. Appellant believes the Examiner is attempting to infer a definition of the input lines and the operation of the FPGA of Larson. However, Appellant submits the inferences being made by the Examiner are unfounded. Any inferences made as to whether the FPGA has some "library" is purely speculation.

More particularly, Larson does not teach any such input line definition as discussed in [0036] and [0061-0064], not does Larson teach the FPGA having any library. Larson never mentions the configuration of the hot-swap status input lines in any other way than there are 18 hot-swap status input lines to the FPGA. Moreover, Appellant submits the hot-swap states discussed and shown in the Intersil HIP1011 document cited by the Examiner are states derived from a number of signal inputs

including the HEALTHY#, ENUM#, PCI_RST#, and BDSEL# signals. In fact, in the Intersil document, there are 7 hot-swap states shown, and not 18. The HEALTHY# and BDSEL# signals are shown in Larson.

Appellant submits Larson teaches the hot-swap status input signals are used by the SMC 300E (the processor) to determine the hot-swap status of a number of various components connected to the hot swap status input lines 522B. Although Larson never states explicitly the use of these hot swap input lines, Appellant theorizes that each of the hot swap lines may be coupled to a respective cards insertion/removal lever, such that the FPGA can generate an interrupt to SMC300E (*See* Larson [0063] above) in response to an attempted removal event.

The Examiner also asserts in the aforementioned final Office action "it is clear that management software is used in conjunction with the system management card 300E, for example, to monitor "BD SEL" and "HEALTHY" and the state of the hotswap is mapped form the FPGA hot-swap status to the hot-swap status of the management software. Appellant disagrees. Specifically, as shown above, Larson merely notes that higher-level management software can self discover and fault manage the system. Appellant fails to see how this anticipates Appellant's claims. Further, Appellant further notes that just because software running on SMC 300E may determine the hot-swap status, it does not mean there is mapping as recited in Appellant's claims. In fact, since Larson teaches the SMC300E may run the higher-level management software instead of the system OS or other software, one could infer that no mapping would be necessary.

For at least the above stated reasons, Appellant submits that the rejection of claim 1 is in error and requests reversal of the rejection. The rejection of claims 3-6 (dependent from claim 1) are similarly in error for at least the above stated reasons, and reversal of the rejection is requested. Each of claims 3-6, 8-9, and 11-23 recite additional features not taught or suggested in the cited art.

For at least the above stated reasons, Appellant submits that the rejection of

claims 7 and 10 is in error and requests reversal of the rejection. The rejection of claims 8-9 (dependent from claim 7), and claims 11-23 (dependent from claim 10) is similarly in error for at least the above stated reasons, and reversal of the rejection is requested. Each of claims 8-9 and 11-23 recite additional features not taught or suggested in the cited art.

For example, claim 10 recites features including: "a manager for managing said CPCI card using **a first management state** and **a second management state**; a common **library** associated with said CPCI node card and said manager, said common library providing an intermediate state; wherein said hot swap state is mapped onto said intermediate state of said common library; and wherein said intermediate state is mapped onto said first and second management states of said manager". Appellant submits these features are not taught or disclosed by Larson as described above.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-23 is erroneous, and reversal of the decision is respectfully requested.

The Commissioner is authorized to charge any fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-10201/SJC. This Appeal Brief is submitted with a return receipt postcard.

Respectfully submitted,

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Date: September 26, 2006

IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. A method of mapping a plurality of states for controlling hot-swappability in a Compact Peripheral Component Interconnect (CPCI) system, said method comprising:

specifying a hot-swap state of a CPCI node card for controlling hot-swappability of said CPCI node card;

mapping said hot-swap state onto an intermediate state by searching a common library associated with said CPCI node card and a management software for said CPCI node card; and

mapping said intermediate state onto a first management state of said management software and a second management state of said management software;

wherein said management software requires both said first and second management states to manage said CPCI node card.

2. The method of claim 1, further comprising:

specifying a second hot-swap state of said CPCI node card for controlling hot-swappability of said CPCI node card;

specifying a transition state of said CPCI node card when said CPCI node card transitions from said first hot-swap state to said second-hot swap state;

mapping said transition state onto an intermediate transition state by searching a common library associated with said CPCI node card.

3. The method of claim 2, further comprising: notifying said management software of said intermediate transition state.

4. The method of claim 3, further comprising the step of mapping said intermediate transition state onto a third management state of said management software and a fourth management state of said management software.

5. The method of claim 4, wherein said first and third management states comprise a first operational state and a second operation state and wherein said second and fourth management states comprise a first availability state and a second availability state.

6. The method of claim 1, further comprising:
representing said CPCI node card as a plug-in unit; and
managing said CPCI node card as said plug-in unit by said management software upon said mapping of said intermediate state onto said first and second management states

7. A method of mapping a plurality of states for controlling hot-swappability in a Compact Peripheral Component Interconnect (CPCI) system, said method comprising:
specifying a PCI Industrial Computer Manufactures Group (PICMG) hot-swap state of a CPCI node card for controlling hot-swappability of said CPCI node card;
mapping said PICMG hot-swap state onto an intermediate state by searching a common library associated with said CPCI node card and a management software for said CPCI node card; and
mapping said intermediate state onto a Telecommunication Management Network (TMN) plug-in unit state of said management software;
wherein said management software requires said TMN plug-in unit state to manage said CPCI node card.

8. The method of claim 7, wherein said common library comprises a Common Operating System Library (COSL) and wherein said intermediate state comprises a COSL state.

9. The method of claim 7, further comprising:
representing said CPCI node card as a TMN plug-in unit; and

managing said CPCI node card as said TMN plug-in unit by said management software upon said mapping of said intermediate state onto said TMN plug-in unit state.

10. A Compact Peripheral Component Interconnect (CPCI) system, comprising:
a CPCI chassis;
a circuit board forming a backplane within said chassis;
a CPCI node card coupled with said circuit board, said node card providing a hot-swap state;
a manager for managing said CPCI card using a first management state and a second management state;
a common library associated with said CPCI node card and said manager, said common library providing an intermediate state;
wherein said hot swap state is mapped onto said intermediate state of said common library; and
wherein said intermediate state is mapped onto said first and second management states of said manager.

11. The CPCI system of claim 10, wherein said manager requires said hot-swap state to be mapped onto said first and second management states via said intermediate state to manage said CPCI node card.

12. The CPCI system of claim 10, wherein said manager manages said CPCI node card as a plug-in unit once said hot-swap state has been mapped onto said first and second management states via said intermediate state.

13. The CPCI system of claim 12, wherein said plug-in unit comprises a Telecommunication Management Network (TMN) plug-in unit.

14. The CPCI system of claim 10, wherein said hot-swap state describes a hot-swap status of said CPCI node card.

15. The CPCI system of claim 10, wherein said first management state comprises an operational state and said second management states comprises an availability state.

16. The CPCI system of claim 15, wherein said operational state comprises one of a null-operational state, an up-operational state, a down-operational state, and an unknown-operational state.

17. The CPCI system of claim 15, wherein said availability state comprises one of a null-availability state, a power-off-availability state, an offline-availability state, an available-availability state, a failed-availability state, and an unknown-availability state.

18. The CPCI system of claim 10, wherein said intermediate state comprises one of a no plug-in state, a first power-off state, a second power-off state, a first unavailable-state, a second unavailable-state, an available state, a failed state, and an unknown state.

19. The CPCI system of claim 10, wherein said hot-swap state comprises a plurality of states for indicating plug-in status.

20. The CPCI system of claim 10, wherein said hot-swap state comprises one of:

a first state for indicating a plug-in unit is present, but not powered on;

a second state for indicating a plug-in unit is powered up, but not connected;

a third state for indicating a plug-in unit is connected;

a fourth state for indicating a plug-in unit is configured, but drivers are not loaded and associated;

a fifth state for indicating a plug-in unit is configured and drivers are loaded and associated;

a sixth state for indicating a plug-in unit is in use; and

two failed states.

21. The CPCI system of claim 10, wherein said manager comprises a management

software having plug-in units based on Telecommunication Management Network (TMN) standard.

22. The CPCI system of claim 21, wherein said hot-swap state comprises a state based on a PCI Industrial Computer Manufactures Group (PICMG) hot-swap/High Availability (HA) specification.

23. The CPCI system of claim 22, wherein said management software manages said CPCI node card as a TMN plug-in unit and requires said hot-swap state to be mapped onto said first and second management states via said intermediate state in order to manage said CPCI node card as said TMN plug-in unit.

X. EVIDENCE APPENDIX

No evidence submitted under 37 CFR §§ 1.130, 1.131 or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings known to Appellant.